IN THE SPECIFICATION:

Please replace the paragraph (Title) that begins on page 1, line 3 with the following amended paragraph.

FABRICATION PROCESS FOR INTEGRATED CIRCUIT HAVING PHOTODIODE DEVICE ~~AND ASSOCIATED FABRICATION PROCESS~~

Please replace the paragraph that begins on page 1, line 7 with the following amended paragraph.

This application is a divisional of application Serial No. 10/044,286, filed January 11, 2002, now U.S. Patent No. 6,670,657, which is based upon and claims priority from prior French Patent Application No. 01-00420, filed January 12, 2001, the entire disclosure of which is herein incorporated by reference.

Please replace the paragraph that begins on page 1, line 24 with the following amended paragraph.

The solution normally used consists in increasing the doping gradient of the junction and the voltage applied to this junction. It is thus possible to obtain a wide space charge region combined with a high junction capacitance. Typically, a voltage of greater than 5 volts must be applied if the doping levels are high. However, current submicron integrated circuits do not allow high voltages to be used ~~since. In~~ since in these technologies, the maximum supply voltage is less than 3.3 volts.

Please replace the paragraph that begins on page 4, line 5 with the following amended paragraph.

According to one embodiment, the substrate is formed from silicon and the capacitive trench includes an internal doped silicon region partially enveloped by an insulating wall laterally separating the internal region from the substrate and surmounted by an upper doped silicon region, this upper region being in contact with the junction. Preferably, the substrate has a highly doped lower part with a p-type conductivity, for example with a dopant concentration of greater than 1018 at/cm^3 (such as a dopant concentration equal to 1019 at/cm^3). The substrate also preferably has an upper part of p-type conductivity, less doped than the lower part. Also preferably, [[The]] the internal region and the upper region of the capacitive trench have an n-type conductivity, and the region of the junction having the n-type conductivity includes a lower region of n-type conductivity in contact with the upper region of the trench, and an upper region of n-type conductivity but more highly doped than the lower region. The use of a highly doped p-type substrate is not required, but it does allow the input resistances and the noise to be reduced.